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Dated: January 19, 2007

Signature:

(Marco Jimenez)

Docket No.: 535352003600
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
CHENG et al.

Application No.: 10/698,257

Filed: October 30, 2003

Art Unit: 2816

For: DIGITAL-TO-ANALOG CONVERTER WITH
ALWAYS-ON CASCODE TRANSISTORS

Examiner: Kenneth B. Wells

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

As required under § 41.37(a), this brief is filed within two months of the Notice of Appeal, which is filed herewith concurrently.

The fees required under § 41.20(b)(2), and any required petition for extension of time for filing this brief and fees therefor, are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

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This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

- I. Real Party In Interest
- II Related Appeals and Interferences
- III. Status of Claims
- IV. Status of Amendments
- V. Summary of Claimed Subject Matter
- VI. Grounds of Rejection to be Reviewed on Appeal
- VII. Argument
- VIII. Claims Appendix
- IX. Evidence Appendix
- X. Related Proceedings Appendix
- Appendix A Claims

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is TelASIC Communications, Inc., the current assignee of the above application.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Current Status of Claims

1. Claims canceled: 1-27, 30-32, 34, 36, and 40
2. Claims withdrawn from consideration but not canceled: none
3. Claims pending: 28, 29, 33, 35, 37, 38, and 39
4. Claims allowed: none
5. Claims rejected: 28, 29, 33, 35, 37, 38, and 39

B. Claims on Appeal

The claims on appeal are claims 28, 29, 33, 35, 37, 38, and 39, of which Claim 28 is an independent claim.

IV. STATUS OF AMENDMENTS

Applicant did not amend the claims in response to the rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention is directed to a high speed, high resolution digital to analog converter (“DAC”).

With reference to Fig. 3 of the present application, a plurality of cascode current output block 52 is used as a unitary switching element (e.g., a unit cell) of a DAC. This is in contrast to the conventional differential pair switching element such as 12 and 14 shown in the DAC of Fig. 1 of the present application.

In accordance with the present invention, the cascode current switch cells employ trickle currents that are placed at the outputs of the switching transistors to keep the cascode transistors in the switching path on a constant “on” state, thereby decreasing the switching time and settling time of the switching transistors, as well as decrease the parasitic capacitance associated with the conventional uncascoded switching elements. In addition, the use of the cascode current switches in a DAC environment provides isolation between the switching transistors and the output summing nodes, thereby further improving the accuracy and dynamic range of the DAC.

A. Summary of Claimed Subject Matter in Independent Claim 28

Claim 28 is directed generally to Fig. 3 of the present application. Specifically, Claim 28 recites a DAC having a first and second summing bus (e.g., 16 & 18 in Fig. 3), a plurality of current switch cells (e.g., 52), each of which includes a first current source (e.g., 20 in Fig. 3) for supplying a first current, a pair of differential transistors (e.g., Q1 & Q2 in Fig. 3), a pair of cascode transistors (e.g., Q_A and Q_B in Fig. 3) having emitters respectively coupled to the collectors of Q1 and Q2 and collectors coupled to the first and second summing buses, and two additional current sources for

supplying trickle currents to the emitters of the cascode transistors (e.g., 56 & 58 in Fig. 3), wherein the trickle currents are 10 to 100 time smaller than the first current of the first current source.

VI. GROUND OF REJECTION TO BE REVIEWED ON APPEAL

Claims 28, 29, 33, 35, and 37-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art in view of Baskett (U.S. patent no. 6,333,672).

VII. ARGUMENT

As discussed in Section V(A) above and illustrated in Fig. 3 of the present application, Claim 28 is directed to a digital-to-analog circuit employing a plurality of current switches, each of which include a cascode circuit having supplied thereto trickle current at the outputs of the switching transistors. As recited in Claim 28, the multiple unit cells are summed together into a load resistor to make up a high-resolution DAC. The use of the cascode circuits with trickle currents as unit cells in a DAC improves the performance of the DAC by providing a faster overall operating speed and improved accuracy, while eliminating parasitic capacitance typically associated with convention DAC architecture using transistors that do not apply the principle of using trickle currents.

The Primary Examiner, in a second final Office Action dated August 29, 2006, rejected Claims 28, 29, 33, 35, and 37-39 under 35 U.S.C. 103(a) as being unpatentable over applicant's prior art (Fig. 1 specifically) in view of Baskett (U.S. patent no. 6,333,672). Applicant respectfully appeal this rejection for the reasons provided below:

Fig. 1 of the present application illustrates a conventional implementation of a DAC. As described in page 4 of the present application, DAC 10 includes a plurality of cells (12, 14) each of which includes a current source (20, 22) and a pair of differential transistors (Q1, Q2 and Q3, Q4).

The DAC includes summing buses (16, 18) connected to ground via load resistance R_L . Fig. 1 of Baskett, on the other hand, illustrate a differential logic circuit 10 for providing pure digital output (i.e., Fig. 1 of Baskett is not directed to a DAC). Specifically, Fig. 1 of Baskett illustrates using a pair of cascode amplifiers (having transistors 12 and 14) with keep alive sources 16 and 18 to reduce voltage variations at nodes 26 and 28 of the differential logic circuit (see col. 1, lines 41-61).

Firstly, Applicants respectfully submit that the admitted prior art, even when combined with Baskett, do not contain any disclosure or suggestion of the DAC recited in Claim 28. Specifically, neither Fig. 1 of the present application nor Baskett contain any disclosure to specify that the trickle currents be 10 to 100 times smaller than a first current from a first current source. Although Baskett discloses at that the keep alive current sources 16 and 18 provide “a nominal amount of current flowing through cascode amplifiers 12 and 14,” (col. 1, lines 52-54), there is no teaching or suggestion of the relative magnitude of the keep alive currents with respect to any other current source.

Furthermore, Applicants respectfully submit that the Examiner did not satisfy his burden of showing motivation to combine Baskett with Fig. 1 of the present application. As the Examiner acknowledged, the admitted prior art does not contain any disclosure of 1) cascode transistors or 2) trickle current sources, as recited in Claim 28; applicants submit that Baskett fails to make up for this deficiency. Although Fig. 1 of Baskett shows transistors 16 and 18 for providing nominal current to “keep alive” transistors 12 and 14, the Primary Examiner did not point to any teachings or disclosure, either within the references themselves (expressly or implicitly) or otherwise provided, that would adequately serve as motivation for one skilled in the art to combine the references in order to reconstruct the invention recited in Claim 28.

As it is well known in the art, there exist many different types of current switches in electrical applications, just as there exist numerous different electrical elements generally that can be used to construct various different circuitry. It is well recognized that a novel combination of elements, even if the elements are known in the art, is patentable. See, e.g., In re Lunsford, 357 F.2d 380, 384 (C.C.P.A. 1966) (citing In re Wright, 268 F.2d 757 (C.C.P.A. 1959)).

At the same time, it is also well settled patent law that hindsight cannot be used as motivation for combining prior art references. See, e.g., Interconnect Planning Corp. v. Feil, 774 F.2d 1132, 1139 (Fed. Cir. 1985) (vacating judgment by trial court, noting it is error to reconstruct the patentee's claimed invention from the prior art by using the patentee's claim as a "blueprint.") (citing Kalman v. Kimberly-Clark Group, 713 F.2d 760, 774 (Fed. Cir. 1983), cert denied 465 U.S. 1026 (1984)). Rather, there must exist some suggestion, teaching, or motivation that would have led a person of ordinary skill in the art to combine the prior art references in a manner claimed. See Graham v. John Deere Co., 383 U.S. 1 (1966); In re Dembiczak, 175 F.3d 994, 998 (Fed. Cir. 1999). To do otherwise, "combining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability -- the essence of hindsight." Dembiczak, 175 F.3d at 999.

In this instance, addressing the issue of motivation to combine the admitted prior art and Baskett, the Primary Examiner, at paragraph 4 of the final Office Action dated August 29, 2006, stated:

"Applicant should carefully reread the grounds of rejection [of the final Office Action dated December 29, 2005] and the teachings of Baskett. The motivation for combining the teaching is clearly set forth therein."

Referring back to paragraph 3 of the final Office Action dated December 29, 2005, the Examiner provided the following in support of motivation to combine the admitted prior art and Baskett:

“The admitted prior art includes all of the limitations of the above-noted claims, except for the limitations of the cascode transistors and the trickle current sources (the recited second and third current sources). Such would have been obvious, however, in view of the teachings of Baskett. In figure 1 of Baskett, note cascode transistors 12 and 14, and also note the trickle current sources 16 and 18. Also note the discussion by Baskett of the benefits of these transistors (thus providing the motivation for one of ordinary skill in the art to add such cascode transistors and trickle current sources to the circuitry shown in instant figure 1).”

Although the Examiner did not point to any specific language in Baskett that discuss “benefits of these transistors,” Applicants believe the Examiner was referring to col. 1, lines 41 to col. 2, line 3 of Baskett:

Referring to FIG. 1, an improved prior art differential logic circuit 10 is illustrated which provides one method of reducing switching delays induced by toggling the conduction states of differential input transistor pairs by using cascode amplifiers. Transistors 12 and 14 provide a cascode amplifier arrangement such that the voltage variation at nodes 26 and 28 is reduced. Reducing voltage variation at nodes 26 and 28 reduces the miller capacitance effect seen at terminals D and D-compliment, which reduces switching delays through prior art differential logic circuit 10. Voltage variation at nodes 26 and 28 can be further reduced by the addition of keep alive current sources 16 and 18. Keep alive current sources 16 and 18 provide a nominal amount of current flowing through cascode amplifiers 12 and 14 regardless of the conduction state of transistors 20 and 22, respectively. Sizing the keep alive current sources 16 and 18 such that current conduction through transistors 16 and 18 is a substantial portion of the total current entering nodes 26 and 28, respectively, the corresponding voltage variation at nodes 26 and 28 can be significantly reduced, thus substantially eliminating the miller effect.

While Baskett indeed discusses the benefits of providing cascode amplifiers and keep alive current sources within a differential logic circuit, which are implemented for pure digital logic purposes, there is no disclosure or suggestion of using such a structure within an analog circuit implementation, including a DAC implementation. In fact, Applicants respectfully submit that it

would be contrary to conventional design wisdom of one skilled in the art, from a digital logic perspective as taught by Baskett, to construct an analog output circuit of the claimed invention by incorporating the pure digital circuitry shown in Fig. 1 of Baskett with that of DAC of Fig. 1 of the present application.

More importantly, the Primary Examiner did not point to any reasons *why* an ordinary artisan would have combined the references to construct the structure recited in Claim 28 of the present application. Instead, the Primary Examiner appears to have taken the position that the Applicants bear the burden of showing a lack of motivation to combine prior art references (see paragraph 4 of the final Office Action dated August 29, 2006). This is not supported by well established law. Indeed, under U.S. patent law, the Examiner bears the initial burden of supporting any *prima facie* conclusion of obviousness. See M.P.E.P. 2142.

In a recent decision, Dystar Textilfarben GmbH & Co. Deutschland KG v. C.H. Patrick Co., the Federal Circuit addressed the proper test for determining whether motivation exist for combining references. 464 F.3d 1356 (Fed. Cir. 2006) (rehearing and rehearing en banc denied). Specifically, the Federal Circuit provided that motivation may be found:

- “ 1) *in the prior art references* themselves;
- 2) in the knowledge of those of ordinary skill in the art that certain references, or disclosures *in those references*, are of special interest or importance in the field; or
- 3) from the nature of the problem to be solved, leading inventors to *look the references* relating to possible solutions to that problem.”

Dystar, 464 F.3d at 1365 (citing Ruiz v. A.B. Chance Co., 234 F.3d 654 (Fed. Cir. 2000) (emphasis in original). The Federal Circuit went on to emphasize that conclusory statements of motivations to combine are “do not fulfill the [PTO’s] obligation to explain all material facts relating to a motivation to combine” Id. at 1366 (citing In re Lee, 277 F.3d 1338, 1341 (Fed. Cir.

2002)). In instances where the cited references do not expressly provide a motivation to combine, the PTO must “explain *why* ‘common sense’ of an ordinary artisan seeking to solve the problem at hand would have led him to combine the references.” Id. at 1366-1367.

In view of the above, Applicants respectfully submit that the Primary Examiner has failed to demonstrate motivation required for combining the cited references. Specifically, the Examiner does not point to any express provision of motivation in the references themselves, point to any evidence suggesting the existence of motivation in the knowledge of the ordinary artisan to combine the references, or nature of problems to be solved such that one skilled in the art would be motivated to look for references relating to possible solutions. Rather, the Examiner simply pointed to Baskett’s discussion of the benefit of implementing cascode transistors and keep alive sources within a differential logic circuit; Applicants submit that such discussions alone do not provide the requisite motivation for combining Baskett and the admitted prior art.

Finally, Applicants submit that, not only is there a lack of motivation to combine Fig. 1 of the present application with Fig. 1 of Baskett, it would be counter intuitive to one skilled in the art to combine the two references. Specifically, as discussed above, Baskett is directed to differential logic circuit to be used for pure digital logic applications. As one skilled in the art can appreciate, digital integrated circuits such as a differential logic gate and analog circuitry are two completely different areas of art. Fig. 1 of Baskett is a logic gate having a two-state digital output (Q and \bar{Q}), where the outputs are located at the collectors of the cascode transistors 12 and 14; the resistors connected to the collectors of the cascode transistors are connected to a common voltage source V_{CC} . Fig. 1 of the present application, on the other hand, is directed to a digital-to-analog converter having multi-level analog outputs, located at resistors R_L , which are connected to common ground.

Applicants submit that one skilled in the art, when looking at these references, even side by side, would not be motivated to combine them since they serve fundamentally different purposes and operate in very different ways. Applicants submit that it is only in hindsight of the present application would one skilled in the art realize the benefit of adding cascode transistors and trick current sources to a multi-cell DAC.

Separately, Applicants submit that the dependent claims of the present application include subject matter that are in of it themselves patentably distinguishable from Baskettt and the admitted prior art. In particular, with respect to Claim 33, neither the admitted prior art nor Baskettt, nor the combination thereof, teach or suggest a buffer transistor connected between the first current source (e.g., 20 in Fig. 3 of the present application) and the common emitters of the differential pair of transistors Q1 and Q2.

Similarly, with respect to Claims 38 and 39, Applicants respectfully submit that neither the admitted prior art nor Baskettt, nor the combination thereof, teach or suggest any of the additional limitations recited in dependent Claims 38 and 39 of the present application.

In view of the above, Applicant respectfully appeals from the Examiner's rejection in the final Office Action dated August 29, 2006.

VIII. CLAIMS APPENDIX

A copy of the claims involved in the present appeal is attached hereto as Appendix A.

IX. EVIDENCE APPENDIX

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the Examiner is being submitted.

X. RELATED PROCEEDINGS APPENDIX

No related proceedings are referenced above, hence no Appendix is included.

Dated: January 19, 2007

Respectfully submitted,

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APPENDIX A

Claims Involved in the Appeal of Application Serial No. 10/698,257:

Claims 1-27 (canceled)

Claim 28 A digital to analog converter comprising:

a first current summing bus;

a second current summing bus; and

a plurality of current switches, each switch including:

 a first current source for supplying a first current;

 a differential pair of transistors adapted to couple said first current to either the first current summing bus or the second current summing bus in response to a pair of complementary input signals;

 a pair of cascode transistors having emitters respectively coupled to the collectors of said differential pair of transistors, and collectors coupled to said first and second current summing buses, respectively; and

 second and third current sources adapted to respectively supply first and second trickle currents to the emitters of said pair of cascode transistors in order to maintain said pair of cascode transistors in an 'on' state regardless of the states of said differential pair of transistors,

 wherein the trickle currents are approximately 10 to 100 times smaller than said first current.

Claim 29 The invention of Claim 28 wherein the bases of said pair of cascode transistors are connected in common to a voltage potential.

Claims 30-32 (canceled)

Claim 33 The invention of Claim 28 wherein each current switch further includes a buffer transistor connected between said first current source and the common emitters of differential pair of transistors.

Claim 34 (canceled)

Claim 35 The invention of Claim 28 wherein said first and second trickle currents are approximately equal.

Claim 36 (canceled)

Claim 37 The invention of Claim 28 wherein each current switch further includes a driver circuit for supplying said pair of complementary input signals.

Claim 38 The invention of Claim 37 wherein said driver circuit includes:

a fourth current source for supplying a fourth current;

a second differential pair of transistors adapted to couple said fourth current to one of the collectors of said second differential pair of transistors in response to a second pair of complementary input signals;

a second pair of cascode transistors having emitters respectively coupled to the collectors of said second differential pair of transistors;

fifth and sixth current sources adapted to respectively supply third and fourth trickle currents to the emitters of said second pair of cascode transistors in order to maintain said second pair of cascode transistors in an 'on' state regardless of the states of said second differential pair of transistors; and

two transistors having bases respectively coupled to the collectors of said second pair of cascode transistors and emitters adapted to output said pair of complementary input signals.

Claim 39 The invention of Claim 38 wherein said fourth current and said third and fourth trickle currents are chosen to generate a low output voltage swing at the emitters of said two transistors having bases respectively coupled to the collectors of said second pair of cascode transistors.

Claim 40 (canceled)